What is claimed is:

1. A flash memory comprising:

a cell region including a gate, a source line, a drain contact, and a cell trench area for device isolation on a silicon substrate; and

a peripheral region positioned around the cell region and including a subsidiary circuit and a peripheral trench area for device isolation on the silicon substrate, wherein the cell trench area of the cell region is shallower than the peripheral trench area of the peripheral region.

2. The flash memory as defined by claim 1, wherein a depth of the cell trench area is between about 1000Å and 2000Å.

3. A method of fabricating a flash memory comprising:

forming a cell region for memory operation and a peripheral region including a subsidiary circuit for memory operation on a silicon substrate;

amorphizing the surface of the cell region by implanting ions into the cell region;

depositing a pad oxide layer and a pad nitride layer in sequence over the cell region and the peripheral region;

forming a photoresist pattern over each of the pad nitride layer in the cell region and the peripheral region;

removing at least a portion of the pad oxide layer and the pad nitride layer through an etching process using the photoresist pattern as a mask, wherein the etching process is stopped when the surface of the substrate in

the cell region is exposed and, at the same time, the substrate in the peripheral region is etched by an appropriate depth;

removing the photoresist pattern; and

performing an etching process using the pad nitride layer etched as a mask so that a relatively shallow cell trench area is formed in the cell region and a relatively deep peripheral trench area is formed in the peripheral region.

4. The method as defined by claim 3, wherein the ion concentration used to perform the ion implantation is between about 1E14 and 5E14.

5. The method as defined by claim 3, wherein the implanted ion is one or Ge and one selected from group IV elements.

6. The method as defined by claim 3, wherein the ion implantation is performed using an inert gas such as Ar, Xe, or Kr.

7. A method of fabricating a flash memory comprising:

forming a cell region for memory operation and a peripheral region including a subsidiary circuit for memory operation on a silicon substrate;

implanting ions into the cell region using As as a dopant for a channel;

depositing a pad oxide layer and a pad nitride layer in sequence over the cell region and the peripheral region;

forming a photoresist pattern over each of the pad nitride layer in both the cell and the peripheral regions; and

removing some parts of the pad nitride layer, the pad oxide layer, and the substrate through an etching process using the photoresist pattern as a mask.

8. The method as defined by claim 7, wherein the implanted As has an energy value between about 25keV and 35keV and the dosage of As is about 1E13.

9. A method of fabricating a flash memory comprising:

forming a cell region for memory operation and a peripheral region for memory operation including a subsidiary circuit on a silicon substrate;

amorphizing the surface of the cell region by implanting ions into the cell region;

depositing a pad oxide layer and a pad nitride layer in sequence over the cell region as well as the peripheral region;

forming a photoresist pattern on each of the pad nitride layer in both the cell and the peripheral regions;

etching the pad nitride layer using an etching solution with a high selectivity of the pad nitride layer to the pad oxide layer;

etching the pad oxide layer using an etching solution with a high selectivity of the pad oxide layer to the silicon substrate; and

etching the silicon substrate using an etching solution with a high selectivity of the silicon substrate to the pad oxide layer.